GROUND SQUIRREL
PERSONAL COMPUTER

PRODUCT SPECIFICATION

(DWG NO-00000000)

TI STRICKLY PRIVATE

SECTION 1

SCOPE

This document defines the product features, system configuration and general physical, electrical, environmental and quality/reliability requirements of the GROUND SQUIRREL Personal Computer.

1.1 PRODUCT STRATEGY

The GROUND SQUIRREL marketing strategy is to provide a low cost, minimal capability computer for the 'first time buyer'. Primary objective is to provide a 'computer literacy' learning aid that will introduce the general consumer (adults and children) to computer programming. Features will be included to allow expansion of the system to provide increased utility, beyond the 'computer literacy' stage. The GROUND SQUIRREL will be designed as a minimal capability member of the TI PERSONAL COMPUTER product line and will be upward compatible relative to user interface, programming language and styling. The GROUND SQUIRREL will be compatible with TI's Low Cost Peripheral product line to provide economical system expansion capability.

The GROUND SQUIRREL will be introduced in countries outside the US and must be competitive in both cost and performance with other systems that will be entering the market. The GROUND SQUIRREL will be UL/CSA approved (as needed) and will meet the requirements of FCC Docket 20780, as a Class B computing device. Also, units to be sold outside of the US, will meet VDE requirements.

1.2 PRODUCT FEATURES

The minimal configuration, of an operational GROUND SQUIRREL Computer system, consists of a console, wall mounted AC adapter, B/W television (with an antenna switch box) and an interface for an audio cassette recorder (user provided). Features of the GROUND SQUIRREL are defined in two categories: (1) features of the CONSOLE and (2) EXPANSION OPTIONS.

1.2.1 CONSOLE. The GROUND SQUIRREL Console will be user programmable in a BASIC language that is a maximized subset of the of the BASIC Language implemented into the TI-99/4A computer system. All BASIC features relating to 99/4A sound, color, sprite, user defined characters and joysticks, will be deleted from the GROUND SQUIRREL BASIC because the hardware of the GROUND SQUIRREL cannot support these functions. Also, the GROUND SQUIRREL will not be compatibile with 99/4A Solid State Software modules. BASIC programs written on audio cassettes will be upward and downward compatible between the GROUND SQUIRREL and 99/4A systems (within the limits of the GROUND SQUIRREL architecture). The console will consist of:

* A 48 key (QWERTY), elastomeric keyboard.
* 2 kbytes of system RAM
* 12 kbytes of system ROM
* TMS-9995 Processor
* Gate Array(s) for Video generation and I/O control functions (to be replaced with a single custom IC as a cost reduction effort)
* RF modulator to generate the B/W video signal for the television (no sound)
* A VHF channel select switch for selecting the video modulation frequency.
* Connections for an audio cassette recorder:
  - Minature phono jack for CASIN (recorder MIC input)
  - Minature phono jack for CASOUT (recorder EAR output)
  - No motor control will be provided (recorder REM input)
* Phono jack for connecting the external wall transformer.
* ALC I/O connector to interface to low cost peripherals.
* System EXPANSION Port will be provided at the rear of the console to allow addition of memory and application software.

1.2.2 EXPANSION OPTIONS. The GROUND SQUIRREL hardware and software systems will be designed to facilitate the expansion of memory (RAM and ROM), addition of applications programs residing in external modules, enhanced peripheral capability and software packages that redefine the functionality of the "operating system". The "redefine" expansions will be utilized to convert the system from a BASIC language tutor to a PASCAL, FORTRAN, etc... learning aid for enhanced computer literacy. The "redefine" option will also facilitate reconfiguration of the system as a low cost terminal. The expansion options are defined as:

* RAM Expansion (up to 32 kbytes) by use of "expansion cradle" that connects to the System Expansion port on the rear of the console. Only on device or module may be connected to the System Expansion port at any time. If an application Software Module is required to run with RAM Expansion, a connector slot will be provided in the RAM Expansion cradle for insertion of the application module.

* Application Software Modules will be designed to connect directly to the system Expansion port (unless the RAM Expansion cradle is used). Modules will contain no RAM, thus, all modules that are used without the RAM Expansion cradle will be limited to the 2 kbytes of system RAM in the console. Application programs will be contained in 4 kbyte multiples of ROM in the modules. The maximum amount of ROM is 48 kbytes without RAM expansion and 16 kbytes if the RAM Expansion cradle is installed.

SECTION 2

APPLICABLE DOCUMENTS

2.1 HARDWARE

* TMS-9995 Microprocessor Data Manual
* TMS-4732/4764 Read Only Memory Specification
* TMS-4016 Random Access Memory Specification
* TI-99/4A Cassette Interface Specification
* CF-40051 CRT Controller Gate Array Specification
* CF-40052 I/O Controller Gate Array Specification
* GROUND SQUIRREL Mechanical Drawing Package
* GROUND SQUIRREL System Hardware Specification
* GROUND SQUIRREL Keyboard Specification
* GROUND SQUIRREL Software Module Specification
* GROUND SQUIRREL RAM Expansion Cradle Specification
* GROUND SQUIRREL ALC I/O Peripheral Bus Specification

2.2 SOFTWARE

* GROUND SQUIRREL System Software Specification
* GROUND SQUIRREL "Learn to Program" Tutor Specification
* TI-99/4A Console BASIC Software Specification

2.3 PERFORMANCE

* National Safe Transit Preshipment Test Procedure
* MIL STD 461A; 462 Methods CS01, CS02, CS06, RS01, RS02 and RS03
* MIL STD 810B
* FCC Rules and Regulations, Part 15, Subparts A, B and H and Part 2 Subpart J
* FCC Docket 20780, Class B, Part 15, Subparts H and J
* UL STD 114
* CSA STD C22.2-154
* VDE STD 380
* JIS STD (tbd)

SECTION 3

GENERAL DESCRIPTION

The GROUND SQUIRREL Computer system will consist of a console (housing the main logic board and keyboard), a B/W television, video cable and antenna switch, audio cassette cable (included), audio cassette recorder (user provided), wall mounted AC adapter, optional RAM Expansion Cradle and Software Modules. A block diagram of the GROUND SQUIRREL system is shown in Figure 3-1.

The Console will be a low profile plastic top case and metal bottom case, containing 2 major subassemblies:

1. Main Logic Board

2. Keyboard assembly

RFI shielding will be provided by the metal bottom case and a metal shield (if required) over the PCB. Appropriate RFI shielding will be employed on all PCB interconnects, external connections and the system expansion port.

The Expansion Module port will be positioned for ease of access to facilitate insertion and removal by the user. The port will be positioned to allow horizontal insertion onto a PCB card edge, eliminating the need for a connector on the console. All connections will be made at the rear of the unit.

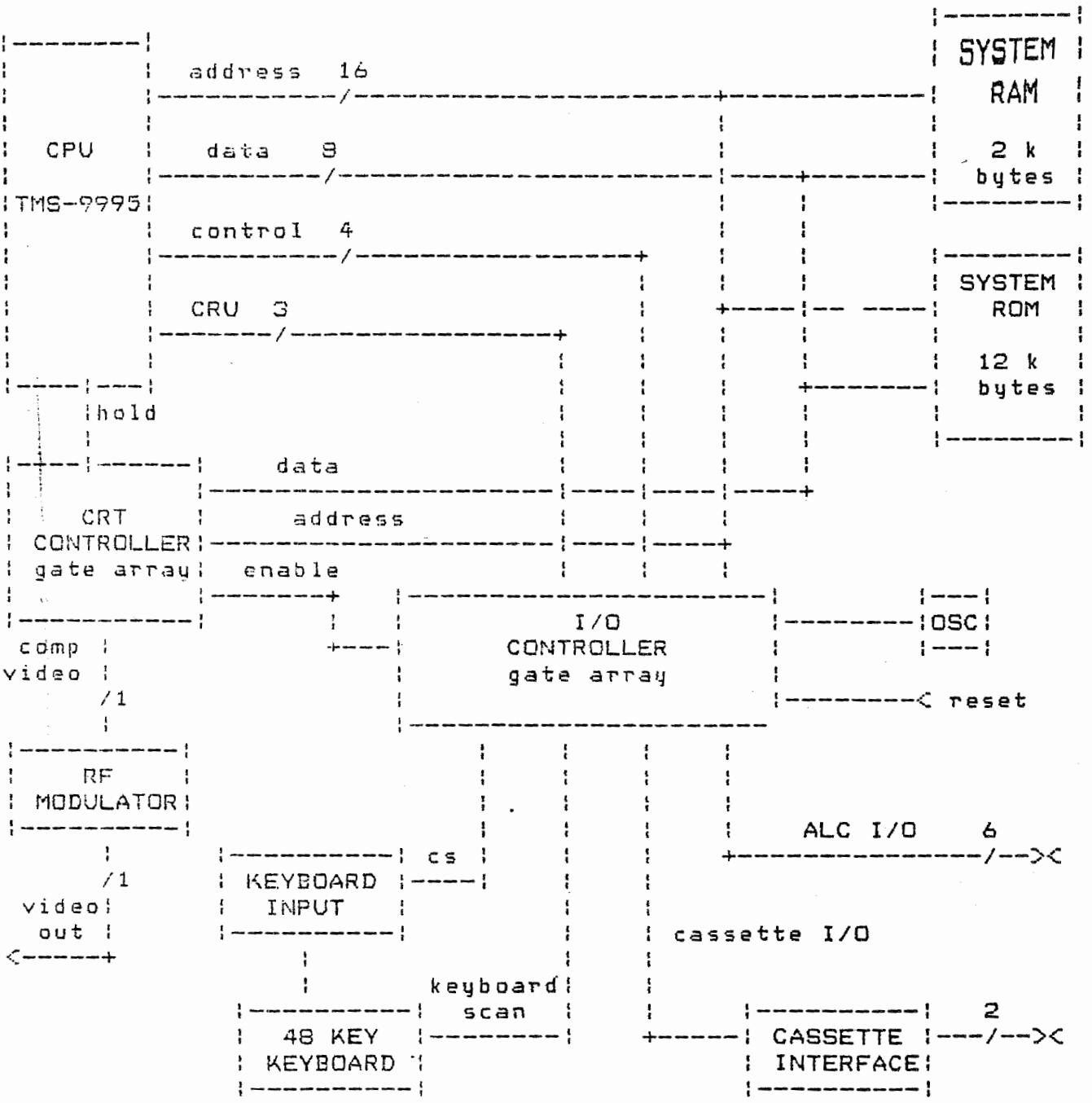

Figure 3-1 GROUND SQUIRREL SYSTEM BLOCK DIAGRAM

3.1 MAIN LOGIC BOARD

The GROUND SQUIRREL will utilize one double-sided PCB as the main logic board of the system. This PCB will contain all of the circuitry for the following functions:

* CPU, ROM/RAM, clock generation, RESET, address decoding and CRU mapping.
* B/W Composite video generation for a 24 row by 32 character display
* ALC I/O Peripheral Interface
* Keyboard interface
* Audio Cassette Recorder interface (single with no motor control)
* System Expansion Port for RAM/ROM expansion and Software Modules
* DC power supply for the system

In order to achieve the "minimal chip" architecture required to satisfy the low cost goals of the product, all memory devices will be 8 bit wide and RAMs will be static devices. All 'random logic' required to generate timing, reset, memory/CRU addressing and peripherial interfacing, will be combined into a TI Gate Array device (I/O Controller) of not more than 40 pins. Logic required to generate the B/W composite video (screen refresh) will be contained in a second 40 pin TI Gate Array device (CRT Controller).

3.1.1 CPU. The GROUND SQUIRREL will utilize the standard TMS-9995 Processor as the central processing unit for the computer. This device is a 16 bit processor with an 8 bit external data bus and has "on-chip" RAM and CRU decodes that must be accomodated in the system memory layout. Figure 3-2 defines both the system memory map and CRU decodes for the GROUND SQUIRREL.

3.1.2 MEMORY.

3.1.2.1 SYSTEM ROM. The GROUND SQUIRREL will have 12 kbytes of system ROM consists of one 8 kbyte ROM (TMS-4764) and one 4 kbyte ROM (TMS-4732). System ROM will be positioned at the low 12 kbytes address space. Refer to Figure 3-2 for the memory map.

3.1.2.2 SYSTEM RAM. System RAM for the GROUND SQUIRREL will be a single 2 kbyte static RAM (TMS-4016). "On-chip" RAM of the TMS-9995 processor (258 bytes) is available such that there will be a total of 2306 bytes of system RAM. The 2 kbyte RAM will be mapped into the address space directly below the CPU "on-chip" RAM to provide contigous RAM space for program storage.

3.1.2.3 PROCESSOR RAM. The 9995 processor has a 252 byte segment of "on-chip" RAM from address >F000 to >F0FB and 6 additional bytes from address >FFFA to >FFFF for "on-chip" register/vector storage.

3.1.2.4 EXPANSION ROM/RAM. Expansion ROM/RAM will occupy the 46 kbytes of address space between system ROM and system RAM. This space may be partioned into ROM and RAM spaces with the constraints that ROM will be in 4 kbyte multiples starting at the boundary of the system ROM and RAM will be in 2 kbyte multiples that are positioned to be contigous with the system RAM. To achieve a full 16 kbyte ROM expansion, 2 k bytes must be mapped into the 3kbyte unused memory segment (refer to section 3.1.2.5). A maximum of 32 kbytes of RAM expansion will be supported.

3.1.2.5 UNUSED MEMORY. Due to the unusual positioning of the "on-chip" RAM/CRU of the TMS-9995 and the address resolution of RAM/ROM addressing (2k/4k byte), there is a 3k byte address space, above the processor "on-chip" RAM, that will not be used. This space will be available for unigue applications if decoded by external circuits.

3.1.3 CRU DECODES. System I/O devices will be CRU based and will be mapped into two major base addresses; one for the keyboard and video enable control signal and one for the ALC I/O bus and audio cassette I/O. Figure 3-2 defines the system level CRU mapping and Table 3-1 identifies the I/O of each CRU base. All CRU lines will be bi-directional except the video enable line which will be an output only.

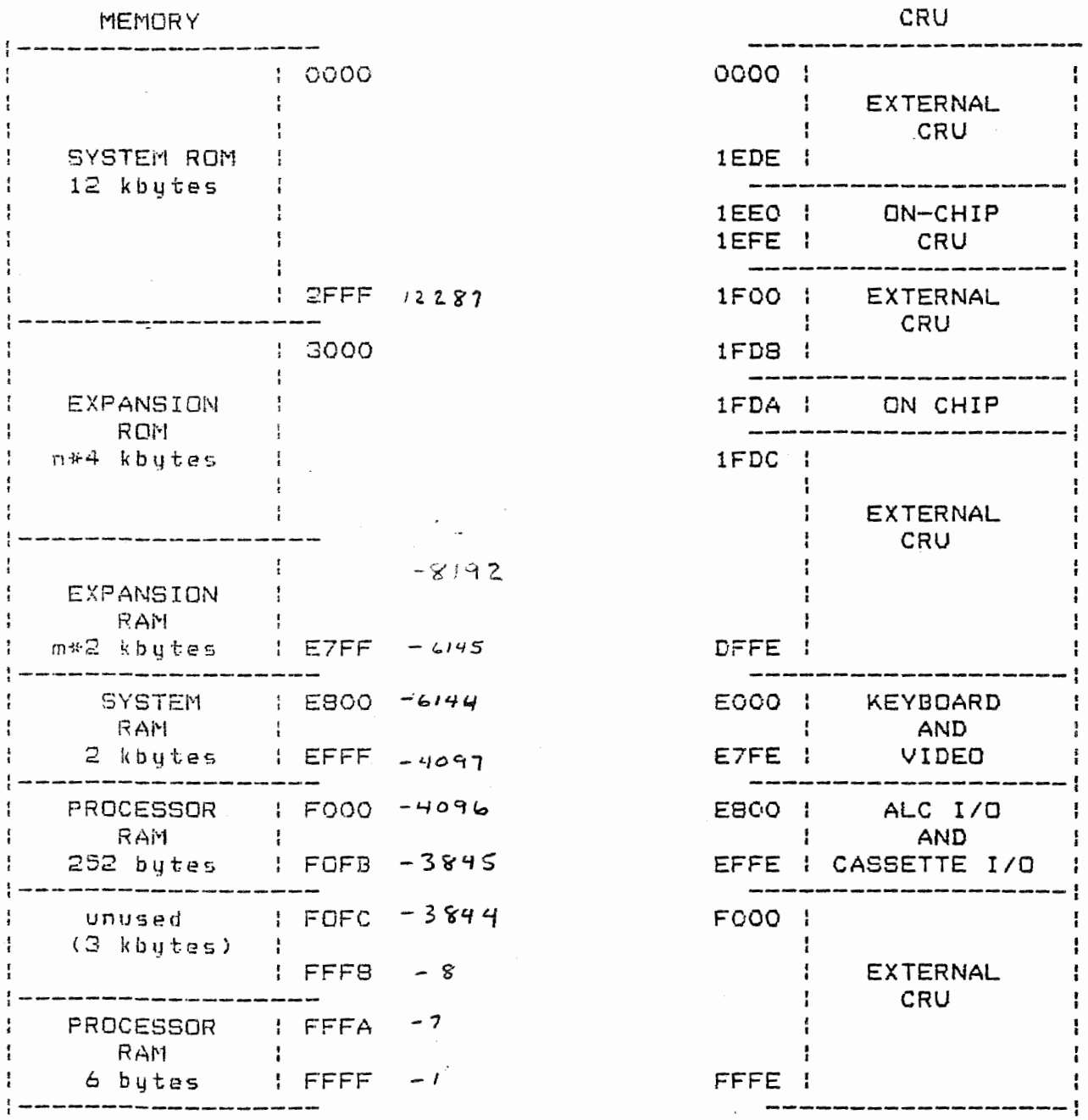

Figure 3-2 MEMORY AND CRU ADDRESS MAPS

Table 3-1 CRU BIT DEFINITIONS

CRUBASE	INPUT		OUTPUT	
>E000	keyboard input COLUMN 0		keyboard output ROW 0	
>E002	" " " 1		" " " 1	
>E004	" " " 2		" " " 2	
>E006	" " " 3		" " " 3	
>E008	" " " 4		" " " 4	
>E00A	" " " 5		keyboard output ROW 5	
>E00C	" " " 6		not used	
>E00E	keyboard input COLUMN 7		video enable (VIDENA)	
>E800	ALC data line	D0	ALC data line	D0
>E802	" " "	D1	" " "	D1
>E804	" " "	D2	" " "	D2
>E806	ALC data line	D3	ALC data line	D3
>E808	ALC handshake	HSK	ALC handshake	HSK
>E80A	ALC bus available	BAV	ALC bus available	BAV
>E80C	not used		ALC inhibit	INH
>E80E	cassette in	CASIN	cassette out	CASOT

3.2 KEYBOARD

The keyboard is a non-interrupt driven, CRU based device with 6 rows and 8 columns to give a total of 48 key stations. The assembly will consist of a mylar key switch matrix on a flex film circuit, with elastomeric keytoppers to provide a tactile feel similar to full travel keyboards. The flex film will connect to the main logic board via a flex film connector.

A 'QWERTY keyboard format will be used and will be functionaly similar to that of the 99/4A console except that the key definitions will be simplified. The GROUND SQUIRREL will use only upper case letters and will have a limited 96 character set. All keys will have no more than 2 definitions per keytop. The normal function keys (DEL, INS, CLEAR, AID, REDO, PROC'D, ERASE, BACK and QUIT) will have the ledgens on the case above the top row of keys. The other function keys (up arrow, down arrow, right and left arrows) will be on the keytops and will respond to either the shift or function keys. Figure 3-3 defines the keyboard layout and the key graphics.

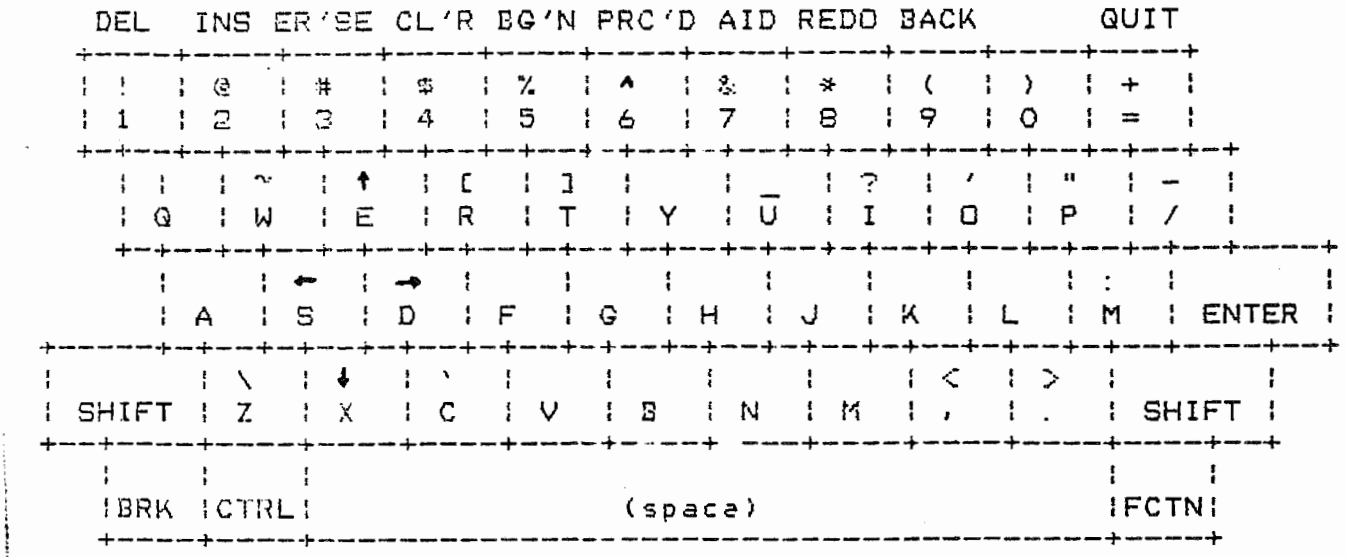

Figure 3-3 KEYBOARD LAYOUT

3.2.1 KEYBOARD INTERFACE. The I/O controller gate array will interface with the keyboard to provide the scan functions. The 6 rows will be the scan inputs (open collector outputs of the I/O Controller gate array) and the 8 columns will be the key matrix outputs. Because of pin limitations on the I/O Controller gate array, the CRU for input from the keyboard will be a separate IC (74LS251) with the enable generated by the gate array. CRU base for the keyboard will be >EF00 through >EF0E.

3.2.2 SCAN METHOD. All rows (scan lines) and columns will be normally "high" (logic one). To scan the keyboard, each scan line will be individually pulled low and the column lines will be read by CRU instructions. If a column line is "low", a key has been detected at the intersection of the row being scanned and the column that is low. Multiple key closures will be detected by this method, however, only the SHIFT, CNTL and FNCT keys are allowed to be pressed at the same time as another key. Any other multiple key closure condition is invalid and only the first key detected will be accepted. Software must provide key debounce logic to eliminate false key entries. Keycode definitions are shown in Figure 3-4.

3.3 VIDEO DISPLAY

The GROUND SQUIRREL will provide RF modulated, composite video for display of a 24 row by 32 character format on a standard B/W television. A channel select switch will be provided to select the correct modulation frequency for either channel 3 or 4 of the VHF band. The CRT Controller gate array will provide the video generation functions. Video display data will be stored in System RAM and the dot patterns for the 96 displayable characters will be stored in System ROM. No special RAM or ROM devices will be utilized.

The video will be 625 line, non-interlaced, for US and 525 line, non-interlaced for the European markets. The CRT Controller gate array will be a separate design for the US and European markets. The RF modulator module will also vary from US to European markets.

3.3.1 VIDEO GENERATION. A DMA type interface will be required to allow the CPU and CRT Controller to utilize the same ROM and RAM devices. CRT Controller will be the 'cycle-steal' device and will use the HOLD line of the TMS-9995 to gain control of the system address and data buses. The CRT Controller will operate from a 10.7 Mhz clock (generated by crystal oscillator on the main logic board) and will supply a 5.35 Mhz clock to the CPU to insure synchronization. The CRT Controller will disable the CPU to refresh each dot line (of each character line) and will release control after the last character is refreshed on that line. This will allow the processor to execute instructions during the screen border display, horizontal retrace and vertical retrace time periods. To maximize the CPU processing time, a BLANK-END-OF-LINE character (BEOL) will be used as the last character of each partioal character line. When the CRT Controller recognizes a BEOL, the system buses will be released and the processor will utilize the remainder of the line as additional compute time. Also, a CRU bit (VIDENA) will be provided that will completely disable the CRT Controller and inhibit all DMA cycles. The screen will be blanked (white) and the CPU will have 100% compute time.

OUTPUT LINES (rows)	MODE	SCAN LINES (columns) 0	1	2	3	4	5
0	function	REDO	BACK		QUIT		ENTER
	shift	*	(	)	+	-	ENTER
	normal	8	9	0	=	/	ENTER
1	function	AID					SHIFT
	shift	&	?	'	"	:	SHIFT
	normal	7	I	O	P	;	SHIFT
2	function	PROC'D					FCTN
	shift	^					FCTN
	normal	6	Y	U	K	L	FCTN
3	function	BEGIN					
	shift	%	]			<	>
	normal	5	T	H	J	,	.
4	function	CLEAR					
	shift	$	[	{	}		
	normal	4	R	F	G	N	M
5	function	ERASE	↑	→			
	shift	#	↑	→	`		
	normal	3	E	D	C	V	B
6	function	INS		←	↓	CTRL	SPACE
	shift	@	~	←	↓	CTRL	SPACE
	normal	2	W	S	X	CTRL	SPACE
7	function	DEL				SHIFT	BREAK
	shift	!			\	SHIFT	BREAK
	normal	1	Q	A	Z	SHIFT	BREAK

Figure 3-4 KEYBOARD DECODES

Video refresh cycle will be initiated by the CRT Controller pulling the HOLD line down and delaying several 'dot' times before taking control of the system busses. A counter chain in the controller will define the character row, column and dot line that is to be refreshed. The CRT Controller will output the counter values plus a bias to adddress the video display RAM area (>EC00 to >EEFF), to determine which character is to be displayed. The data at the RAM location is appended to the character pattern ROM base address (>1C00) and the dot line count, to address the appropriate byte in the character pattern ROM. Data from the ROM is loaded into an 8 bit shift register to generate the composite video.

3.3.2 VIDEO SCREEN RAM. The 24 rows of 32 characters are stored in system RAM (video RAM buffer) starting at address >EC00 and continuing to >EEFF (768 bytes). The next byte (>EF00) is the screen attritubute control byte. Figure 3-5 defines the character set to be implemented.

3.3.3 CHARACTER PATTERN ROM. Dot patterns for each of the 96 displayable characters are stored in system ROM (CHARPAT) starting at address >1C00 and extending to >1EFF for a total of 768 bytes (96 times 8). Figure 3-6 defines the character patterns.

3.3.4 SCREEN ATTRIBUTE CONTROL. The byte immediately following the video display RAM (>1F00) is used to control the screen attributes relative to border and screen/character color. The bit definitions are as follows (B0 is the LSB):

B7-B3	B2	B1	B0
not used	screen color 1 = black	border color 1 = white	reserved for future use

3.3.5 BLANK-END-OF-LINE CONTROL. Any character code greater than >70 will be used as a Blank-End-Of-Line (BEOL) character which will stop the controller from refreshing the remainder of the line and relenquish control of the address and data buses. The BEOL feature will be used on all non-full display lines to provide more compute time for the CPU. Also, writing a >7X into the first character of a line will blank the line on the screen, however the video RAM is not cleared. Video may be fully disabled by setting the VIDENA CRU bit to a low.

CODE (hex)	CHAR	CODE (hex)	CHAR	CODE (hex)	CHAR
00		26	&	4C	L
01		27	'	4D	M
02		28	(	4E	N
03		29	)	4F	O
04		2A	*	50	P
05		2B	+	51	Q
06		2C	,	52	R
07		2D	-	53	S
08		2E	.	54	T
09		2F	/	55	U
0A		30	0	56	V
0B		31	1	57	W
0C		32	2	58	X
0D		33	3	59	Y
0E		34	4	5A	Z
0F		35	5	5B	[
10		36	6	5C	\
11		37	7	5D	]
12		38	8	5E	^
13		39	9	5F	
14		3A	:	60	
15		3B	;	61	
16		3C	<	62	
17		3D	=	63	
18		3E	>	64	
19		3F	?	65	
1A		40	@	66	
1B	{	41	A	67	
1C	|	42	B	68	
1D	}	43	C	69	
1E	~	44	D	6A	
1F	`	45	E	6B	
20	space	46	F	6C	
21	!	47	G	6D	
22	"	48	H	6E	
23	#	49	I	6F	
24	$	4A	J	70--FF	BEOL
25	%	4B	K	(blank-end-of-line)	

Figure 3-5 DISPLAY CHARACTER SET

CODE	PATTERN	CHAR	CODE	PATTERN	CHAR
00	0000, 1000, 1000, 1000	⋮	38	0038, 4444, 3844, 4438	8
01	0000, 0000, 5400, 0000	⋯	39	0038, 4444, 3C04, 0830	9
02	3C42, 8199, 9981, 423C	⊙	3A	0000, 3030, 0030, 3000	:
03	3C42, A599, 99A5, 423C	⊗	3B	0000, 3030, 0030, 1020	;
04	0040, 2010, 7840, 2010	≈	3C	0008, 1020, 4020, 1008	<
05	8142, 2418, 1824, 4281	X	3D	0000, 007C, 007C, 0000	=
06	8040, 2010, 0804, 0201	\	3E	0020, 1008, 0408, 1020	>
07	0102, 0408, 1020, 4080	/	3F	0038, 4404, 0810, 0010	?
08	0000, 0000, 1F10, 1010	⌐	40	0038, 445C, 545C, 4038	@
09	1010, 1010, 1F00, 0000	⌙	41	0010, 2844, 447C, 4444	A
0A	1010, 1010, F000, 0000	⌐	42	0078, 2424, 3824, 2478	B
0B	0000, 0000, F010, 1010	⌙	43	0038, 4440, 4040, 4438	C
0C	0000, 0000, FF00, 0000	─	44	0078, 2424, 2424, 2478	D
0D	1010, 1010, 1010, 1010	┤	45	007C, 4040, 7840, 407C	E
0E	1010, 1010, FF00, 0000	┴	46	007C, 4040, 7840, 4040	F
0F	0000, 0000, FF10, 1010	┼	47	003C, 4040, 5C44, 4438	G
10	1010, 1010, F010, 1010	┤	48	0044, 4444, 7C44, 4444	H
11	1010, 1010, 1F10, 1010	├	49	0038, 1010, 1010, 1038	I
12	1010, 1010, FF10, 1010	┼	4A	0004, 0404, 0404, 4438	J
13	2854, 4444, 4428, 2810	♡	4B	0044, 4850, 6050, 4844	K
14	1028, 2844, 4444, 5428	△	4C	0040, 4040, 4040, 407C	L
15	0000, 7886, 4186, 7800	▷	4D	0044, 6C54, 5444, 4444	M
16	0000, 1E61, 8261, 1E00	◁	4E	0044, 6464, 544C, 4C44	N
17	0000, 1020, 7C20, 1000	←	4F	007C, 4444, 4444, 447C	O
18	0000, 1008, 7C08, 1000	→	50	0078, 4444, 7840, 4040	P
19	0000, 1038, 5410, 1000	↑	51	0038, 4444, 4454, 4834	Q
1A	0000, 1010, 5438, 1000	↓	52	0078, 4444, 7850, 4844	R
1B	0018, 2020, 4020, 2018	(	53	0038, 4440, 3804, 4438	S
1C	0010, 1010, 0010, 1010	¦	54	007C, 1010, 1010, 1010	T
1D	0030, 0808, 0408, 0830	)	55	0044, 4444, 4444, 4438	U
1E	0000, 2054, 0800, 0000	~	56	0044, 4444, 2828, 1010	V
1F	0000, 2010, 0800, 0000	`	57	0044, 4444, 5454, 5428	W
20	0000, 0000, 0000, 0000	space	58	0044, 4428, 1028, 4444	X
21	0010, 1010, 1010, 0010	!	59	0044, 4428, 1010, 1010	Y
22	0028, 2828, 0000, 0000	"	5A	007C, 0408, 1020, 407C	Z
23	0028, 287C, 287C, 2828	#	5B	0038, 2020, 2020, 2038	[
24	0038, 5450, 3814, 5438	$	5C	0000, 4020, 1008, 0400	\
25	0060, 6408, 1020, 4C0C	%	5D	0038, 0808, 0808, 0838	]
26	0020, 5050, 2054, 4834	&	5E	0000, 1028, 4400, 0000	^
27	0008, 0810, 0000, 0000	'	5F	0000, 0000, 0000, 007C	_

Figure 3-6 CHARACTER PATTERNS

CODE	PATTERN	CHAR	CODE	PATTERN	CHAR
28	0008,1020,2020,1008	(	60	FF81,8181,8181,81FF	
29	0020,1008,0808,1020	)	61	FFFF,FFFF,FFFF,FFFF	
2A	0000,2810,7C10,2800	*	62	F0F0,F0F0,0000,0000	
2B	0000,1010,7C10,1000	+	63	0F0F,0F0F,FFFF,FFFF	
2C	0000,0000,0030,1020	,	64	0F0F,0F0F,0000,0000	
2D	0000,0000,7C00,0000	-	65	F0F0,F0F0,FFFF,FFFF	
2E	0000,0000,0000,3030	.	66	0000,0000,0F0F,0F0F	
2F	0000,0408,1020,4000	/	67	FFFF,FFFF,F0F0,F0F0	
30	0038,4444,4444,4438	0	68	0000,0000,F0F0,F0F0	
31	0010,3010,1010,1038	1	69	FFFF,FFFF,0F0F,0F0F	
32	0038,4404,0810,207C	2	6A	F0F0,F0F0,0F0F,0F0F	
33	0038,4404,1804,4438	3	6B	0F0F,0F0F,F0F0,F0F0	
34	0008,1828,487C,0808	4	6C	F0F0,F0F0,F0F0,F0F0	
35	007C,4078,0404,4438	5	6D	0F0F,0F0F,0F0F,0F0F	
36	0018,2040,7844,4438	6	6E	FFFF,FFFF,0000,0000	
37	007C,0408,1020,2020	7	6F	0000,0000,FFFF,FFFF	

Figure 3-6 CHARACTER PATTERNS cont'd

3.4 AUDIO CASSETTE INTERFACE

The audio cassette interface will be a CRU mapped I/O system. Analog interface circuits will be functionally equivalent to that of the 99/4A system. Software to implement the cassette I/O will also be functionally equivalent in order to insure compatibility of {@%} and {@&} cassette tapes.

3.4.1 CRU BASE. The CRU address of the cassette I/O will be at >E80E and will be a bidirectional port.

3.4.2 DATA ENCODE/DECODE. Data will be encoded as binary '1' and '0' on the cassette tape using a pulse /width modulation technique. Since the cassette media for the {@%} must be compatible with the TI-99/4A system, the software for the encoding should be as specified by the TI-99/4A BASIC Interpreter specification.

3.5 ALC I/O PORT

The ALC I/O Port will be used by the GROUND SQUIRREL console as a printer port, to access a low cost printer system that is compatible with the ALC I/O system. The port will be CRU mapped I/O and will be implemented on the I/O Controller gate array. Refer to the ALC I/O Perirpheral Bus Specification for details of implementation.

3.5.1 CRU BASE. CRU base address for the ALC I/O will be at >E800 to >E80C. The first 6 CRU bits will be bi-directional. The 7th bit (>E80C) will be the message inhibit bit (INH) and will be an output only. The INH will serve two functions:

* When INH is low, normal ALC I/O functions will be allowed. When INH is a one, all data lines, handshake and bus available functions will be disabled.

* INH may be toggled low-high-low as a 'message ignore' indication. After a frame has been initiated by some device on the line, other than the GROUND SQUIRREL, software will read the Device ID byte sent by the requesting device. If the ID does not match the GROUND SQUIRREL, toggling the INH bit will prevent the ALC I/O port from responding to any more nibbles (i.e. handshakes) until the next message frame, as signified by the falling edge of BAV.

3.6 POWER SUPPLY

The Power Supply Assembly for the GROUND SQUIRREL will consist of the following:

* An external, wall mounted AC transformer/full wave bridge rectifier assembly and a cable with a phono plug

* PCB circuit with filter capacitor and a linear regulator (78M05) to convert unfiltered 10 Vdc to 5 Vdc at approximately 1.0 amps.

No Power ON/OFF switch will be used. Power may only be cycled by disconnecting and connecting the power cable. Heat sinking will be provided to keep the temperature of the components within recommended operating ranges.

Selection of the components for the regulator circuit will comprehend the 50 to 60 Hz range to insure ECD compatibility.

Adaptation to the various line voltages (100, 110, 120, 200, 220 and 240 (+/-10%) VAC) for ECD compatibility, will require a different external transformer.

3.7 EXPANSION PORT

The optimum set of system bus level signals will be presented to the exterior of the console at the System Expansion Port. Signals required include the system address/data/control and CRU buses, CPU clock, reset and CRT Controller horizontal/vertical sync signals (to facilitate the use of dynamic RAMS for memory expansion) and the video enable line (wire OR'ED to allow external video disable). Modules attached to the expansion port will buffer all lines to prevent bus loading. A male, 60 pin card edge connection will be provided at the expansion port and the modules will have the 60 pin mating connector.

3.8 SOFTWARE

System Software for the GROUND SQUIRREL will be a maximized subset of the 99/4A Console Basic system. Refer to the GROUND SQUIRREL Software Specification for details. In general, the system software supervisor will be writen in 9995 assembly language and will provide for user interface, peripherial access and control, Expansion port interface, keyboard interface, user application program execution and video generation.

3.9 FUNCTIONAL

3.9.1 POWER-UP. At power application, system software will execute code to initialize all hardware. The system will identify available RAM and then all ROM based user application programs. Video will be disabled to provide a blank (white) screen.

With resources identified, the system initializes default values, builds a MENU of available user applications and then enables video to display the MENU and prompt user action.

3.9.2 EXECUTION. After the user selects an application, system software will begin execution of the package. System software will supply user input controls, via the keyboard, for a 'BREAK' function.

3.10 PHYSICAL REQUIREMENTS

3.10.1 CONSOLE. The GROUND SQUIRREL system Console will be a low profile package (compatible with other TI Personal Computer product styling) consisting of:

* Plastic top case
* Metal bottom case
* Possible metal 'Middle Case' assembly that will serve as the RFI shield for the electronics in the system. The top and bottom cases will be slotted in appropriate areas to provide venting for the heat generated by the system. NO cooling fan will be provided. Sufficient venting will be provided to allow operation to 20 deg C above ambient without degradation of reliability.

Dimensions of the Console will be (design goals):

- Length: 9.5 inches
- Width : 10.0 inches
- Heigth: 1.5 inches

Weight of the fully assembled Console (less Language and Memory Expansion cards) will be less than 1.0 pounds.

3.10.2 KEYBOARD. The keyboard will provide 48 key stations in a staggered key, 4 row arrangement similar to that of the 99/4A system except for deletion of lower case letters which allows elimination of graphics on the front of keys and repositioning of several key ledgens. The keyboard will utilize a mylar film key switch matrix and flexible plastic (i.e. elastomeric) keytops to provide a tactile feel similar to a "full travel" key switch. Design of the elastomeric keytops must provide an expected life of more than 3 million cycles per key. Refer to the 99/4A Keyboard Specification for details.

3.10.3 SOLID STATE SOFTWARE MODULE. Form factor will be similar to the existing 99/4(A) Solid State Software Command Modules (but will not be interchangeable) and will be designed for vertical positioning on the back of the console using a right angle connector. The modules will consist of 2 plastic pieces, a female card edge connector and a PCB capable of supporting 6 74LSXX (16 pin) devices for buffering and 2 ROM devices in 24 pin packages. Dimensions of the module will not exceed 4.5"x3.0"x1.2".

3.10.4 OPTIONS. The RAM Expansion Cradle will be enclosed in plastic package and will be physically attached to the bottom side of the console with a 'neck' extending up to connect to the System Expansion port. A secondary port will be provided, on the back of the cradle, for connecting to Software Modules. The cradle will consist of a 60 pin card edge connector and a PCB large enough for 10 74LSxx devices (16 pins), 8 dynamic RAMs (24 pins) and 1 ROM (24 pins)

3.10.5 INTERCONNECTS. The GROUND SQUIRREL system requires 6 external connections:

* MODULATED VIDEO output = RCA Phone jack
* CASSETTE recorder = minature phono jacks (2)
* SYSTEM EXPANSION PORT = 60 pin, PCB Card Edge (no connector)
* ALC I/O PORT = 8 pin, male
* POWER INPUT = phono jack

3.10.6 SWITCHES. Only one switch will be required on the console; a SPDT slide switch to select the proper channel frequency for the RF modulator. An external antenna switch will be required to allow user selection of the computer video or standard TV signals without having to disconnect the unit.

SECTION 4

MANUFACTURING CONSIDERATIONS

4.1 COMPONENTS

Primary objective will be to design the system to utilize existing production electronic components and mechanical parts to the maximum extent possible. Also, component selection will consider the should be from components that have been qualified by TI Consumer Product Group. These considerations will facilitate qualification, manufacturing planning/material handling and purchasing agreements.

4.2 ASSEMBLY

All aspects of the system design, tooling and assemble equipment development will be targeted toward a "zero-labor" goal. System electronic and mechanical design will be directed toward manufacture by auto sequence/insert techniques. Circuitry and components requiring 'hand-stuff' operations will be minimized. All components should be compatible with wave solder and wash operations. System design will comprehend test and TS&R requirements. Assembly operations will utilize 'snap-together' parts to the maximum degree possible.